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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,847	02/11/2002	Matthias Stecher	WMP-IFT-699	6635

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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,847	STECHER ET AL.	
	Examin r	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on th cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8,10,11 and 13* is/are rejected.

7)☒ Claim(s) *3, 4, 9, 12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the response filed on April 15, 2004.

Claims 1, 2, 5, 6, 8, 10, 13 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira (United States Patent 6,097,063, already of record) together with Letavic et al. (United States Patent 6,221,737 – hereafter Letavic – already of record) and Assaderaghi et al. (United States Patent 6,121,661 – hereafter Assaderaghi – already of record).

With respect to independent claim 1, Fujihira discloses a semiconductor component (see the entire reference, particularly Fig. 6), comprising: a semiconductor substrate 5; an insulation layer 6 on said semiconductor substrate, said insulating layer having an unspecified thickness; a semiconductor layer configured on said insulation layer; a first doped terminal zone 9 and a second doped terminal zone 8 formed in said semiconductor layer; and a drift zone 190 formed in said semiconductor layer; said drift zone formed between said first doped terminal zone and said second doped terminal zone, said drift zone including a plurality of complementary doped adjacent sections 1 and 2.

There are two differences between Fujihira's semiconductor component and claim 1's semiconductor component.

The first difference between Fujihira's semiconductor component and claim 1's semiconductor component is the insulating layer of claim 1's silicon-on-insulator (SOI) structure has a thickness of between 50 nm and 200 nm (Fujihira does not disclose the thickness of its analogous insulating layer 6).

The second difference between Fujihira's semiconductor component and claim 1's semiconductor component is at least one of claim 1's first and second doped terminal zones directly adjoins the semiconductor substrate.

With respect to the first difference, Letavic teaches that the insulating layer of a power SOI structure is typically 100 nm to 5000 nm (see the paragraph bridging columns 3 and 4).

It would have been obvious to one skilled in this art to form Fujihira's layer 6 100 nm to 5000 nm thick because Letavic teaches that a power SOI structure's insulating layer typically has such a thickness.

With respect to the second difference, Assaderaghi teaches connecting an SOI MOSFET's source and drain regions to the underlying semiconductor substrate in order to provide ESD (electrostatic discharge) protection and improved heat dissipation (see the entire reference, particularly Fig. 4A).

It would have been obvious to one skilled in this art to connect Fujihira's drain and source regions 9 and 8 (i.e., its first and second doped terminal zones) to underlying substrate 5 in order to provide Fujihira's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi.

Claim 1 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 2, as stated above with respect to independent claim 1, it would have been obvious to one skilled in this art to connect Fujihira's drain and source regions 9 and 8 (i.e., its first and second doped terminal zones) to

underlying substrate 5 in order to provide Fujihira's semiconductor component with ESD protection and improved heat dissipation, as taught by Assaderaghi.

Claim 2 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 5, Fujihira's semiconductor component further comprises a depletion zone 7 configured between said second terminal zone 8 and said drift zone 190; said depletion zone having a (p) conduction type; and said first terminal zone 9 and said second terminal zone 8 having a conduction type (n) that is complementary to said conduction type of said depletion zone.

Claim 5 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent clam 6, Fujihira's first terminal zone 9 has a (n) conduction type; and its drift zone 1(190) (see Fig. 6B) has a (n) conduction type that is equivalent to the conduction type of said first terminal zone.

Claim 6 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 8, Fujihira's plurality of complementary doped adjacent sections includes first sections 1 and second sections 2; said first sections 1 and said first terminal zone 9 are of a first (n) conduction type; said first sections are connected to said first terminal zone; said second sections 2 and said depletion zone 7 are of a second (p) conductivity type complementary to said first conduction type; and said second sections are connected to said depletion zone.

Claim 8 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 10, Fujihira's plurality of complementary doped adjacent sections 1 and 2 run in a longitudinal direction between first terminal zone 9 and said second terminal zone 8.

Claim 10 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 13, Fujihira's semiconductor component comprises a depletion zone 7 configured between the second terminal zone 8 and the drift zone 190; the plurality of complementary doped adjacent sections 1 and 2 running between the first terminal zone 9 and the depletion zone 7.

Claim 13 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

With respect to dependent claim 11, Fujihira's plurality of complementary doped adjacent sections includes first sections 1 and second sections 2; said first sections 1 and said first terminal zone 9 are of a first (n) conduction type; said first sections are connected to said first terminal zone; said second sections 2 and said depletion zone 7 are of a second (p) conductivity type complementary to said first conduction type; and said second sections are connected to said depletion zone.

Claim 11 is thus rejected under 35 U.S.C. §103(a) as being unpatentable over Fujihira together with Letavic and Assaderaghi.

Claim 3 is objected to as being dependent on a rejected base claim (i.e., claim 3 would be allowable over the prior art of record if claim 3 were amended to further include all the limitations of independent claim 1 and dependent claim 2).

Claim 4 is objected to as being dependent on a rejected base claim (i.e., claim 4 would be allowable over the prior art of record if claim 4 were amended to further include all the limitations of independent claim 1).

Claim 9 is objected to as being dependent on a rejected base claim (i.e., claim 9 would be allowable over the prior art of record if claim 9 were amended to further include all the limitations of independent claim 1).

Claim 12 is objected to as being dependent on a rejected base claim (i.e., claim 12 would be allowable over the prior art of record if claim 12 were amended to further include all the limitations of independent claim 1 and dependent claim 10).

Claim 14 is objected to as being dependent on a rejected base claim (i.e., claim 14 would be allowable over the prior art of record if claim 14 were amended to further include all the limitations of independent claim 1).

The applicant's argument is not persuasive. Specifically, the applicant's premise: "The SOI component as shown in Figs. 6A-6C of Fujihira should have a breakdown voltage of 100 V (see column 12, line 4). Fujihira does not disclose how thick the insulation layer 6 should be in order to reach such a breakdown voltage. However, a person skilled in the art would know that the thickness of the insulation layer in the SOI component of Fujihira must be clearly more than 200 nm in order to reach a breakdown voltage of 100 V," is flawed because Fujihira discloses that 100 V is merely an "ideal"

breakdown voltage (see column 12, line 4). Indeed, the applicant admits: "the voltages that occur in power components are usually between 10 V and 100 V or more" (see the specification at page 2, lines 22-24). Thus even assuming for the sake of argument that the applicant is correct in stating: "it is well known to a person skilled in the art that a breakdown voltage of 100 V requires the thickness of the insulation layer to be more than 250 nm," such is not dispositive because Fujihira's SOI power component's breakdown voltage is not limited to 100 V, but is between 10 V and 100 V or more (which is consistent with Letavic's teaching that an SOI power component's insulating layer is typically 100 nm to 5000 nm).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner